TSMC-03-268

January 22, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/700,779 11/04/03

An-Chun Tu et al.

METHOD FOR IMPROVING INTERLEVEL DIELECTRIC GAP FILLING OVER SEMI-CONDUCTOR STRUCTURES HAVING HIGH ASPECT RATIOS

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 1/27/04

U.S. Patent 5,751,040 to Chen et al., "Self-Aligned Source/Drain Mask ROM Memory Cell Using Trench Etched Channel," describes a method for forming vertical FETs for ROM memory cells in which a source is formed in a trench, an FET channel is formed in the trench wall, and a drain on the surface which are self-aligned.

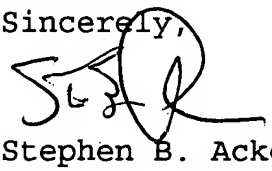
U.S. Patent 4,994,404 to Sheng et al., "Method for Forming a Lightly-Doped Drain (LDD) Structure in a Semiconductor Device," discusses using a disposable amorphous carbon sidewall spacer to self-align the souce/drain contacts to the LDD.

U.S. Patent 6,380,535 to Wetzel et al., "Optical Tuft for Flow Separation Detection," describes a method for making side-wall spacers on an FET gate electrode without damaging the substrate during etching.

U.S. Patent 6,455,373 to Pham et al., "Semiconductor Device Having Gate Edges Protected from Charge Gain/Loss," discusses making flash memory (floating gate) FETs in which the sidewalls are of different thicknesses on the source and drain sides to reduce leakage currents, such as ion charge and the like.

U.S. Patent 6,365,943 to Gardner et al., "High Density Integrated Circuit," describes a method for making two levels of FET devices to increase circuit density on the chip.

Sincerely,



Stephen B. Ackerman,
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Sheet 1 of 1

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
TSMC-03-268	10/700,779
Applicant: An-Chun Tu et al.	
Filing Date: 11/04/03	Group Art Unit

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5751040	5/12/98	Chen et al.	257	332	9/16/96
	4994404	2/19/91	Sheng et al.	437	44	8/28/89
	6365943	4/2/02	Gardner et al.	257	377	9/21/98
	6380535	4/30/02	Wetzel et al.	250	227.14	8/6/99
	6455379	9/24/02	Pham et al.	438	257	4/12/01

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.